EDUCATIONAL MICROPROCESSOR SYSTEM WITH PENTIUM – CPU CARD

The article presents specific requirements regarding the cooperation of a microprocessor Pentium P5 100 MHz with a VMEbus used in the Microprocessor Technique Laboratory for students of Electronics and Telecommunications discipline within the EAIIE Department of the University of Science and Technology (AGH). Particular attention has been paid to the presentation of effective bus access solutions and the method of signal conversion. An explanation on how to reconcile Intel microprocessor requirements partially contradicting each other with Motorola bus standards is also given.

Keywords: microprocessor system, Pentium CPU card, VMEbus standard, microprocessor laboratory stand

1. INTRODUCTION

The purpose of constructing this card was to get students acquainted with the operation of Pentium microprocessors (Pentium P5 100 MHz was used). Such conditions are not met by any PC-computer mainboard where the processor is adapted to a specific configuration and a high integration level precludes inspection of individual signals. It was decided to create a card for an open system. The use of VME standard was as it were forced upon us since all microprocessor systems present in educational laboratories use this standard which in turn enables utilisation of typical modules created for purposes of other systems [1].

In order to achieve the educational aim an attempt was made to demonstrate as complete set of microprocessor actions as possible and to give maximum visual transmission. Whereas operating speed was not a significant parameter due to economic considerations, the lowest allowable clock frequency - 25 MHz was used (still acceptable to Pentium P5) so that only a four layer PCB would be suitable for the task. Such a number of layers still enable retouching which is unavoidable in prototype construction.

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Figure 1 presents a block diagram of the card. Bus access and cycle state machine are distinguished. Cycle state machine manages an extensive buffer set, reconfiguring transfer format. Interrupts logic is necessary for earlier cards (80386, 80486) used in our laboratory. It has already been presented in [2]. It should also be stated that full functional – signal compatibility between the microprocessor (Intel) and the bus (Motorola) cannot be achieved. The problem which cannot be ultimately solved is the lack of general obligatory binary equalization in Intel microprocessors, which has been neglected at the very beginning of the evolution line. Despite substantial inconsistencies, requirements of VME standard [3] have been kept to.

The signals specific to the microprocessor were visualised by means of LEDs (outputs) or provided with pushbuttons with rebound suppressors (inputs). Parity logic, which does not contribute anything to the system, was completely abandoned. Multiprocessor run lines are inactive so that the embedded APIC system is not activated. The card was however equipped with a proprietary test connector and there was also a connector of JTAG standard port on the front panel.

2. BUS ACCESS STATE MACHINE

A bus arbiter assigns access to the bus for each MASTER type card. It is not usually possible to directly connect signals “suspending” the microprocessor to arbitration so that intermediate systems are installed on the card. For obvious
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reasons these are not programmable systems but hardware state machine usually timed with the same clock that serves microprocessor (µp) timing. If identical µp timed with a common clock are using a common bus, then bus handing over can be done without loosing the clock cycle. This applies to such µp which “normally” do not use a bus. The given µp “requests” bus assignment from the bus arbiter and carries out proper cycles after reception and then “releases” the bus which in turn can be assigned to another µp which is waiting for it. Intel microprocessors do not belong to this group. In this case the arbiter must “take the bus away” from all µp except the one which will use it. This finds its reflection in access state machine operations network which was further adapted to atypical situations specific to educational conditions (figure 2).

![Operations network of bus access state machine](image)

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Fig. 2. Operations network of bus access state machine
In the case of processors that normally use a bus, instruction on a specific level of requests of more than one processor forces the extension of the state machine with timing circuits, controlling logic of chain acknowledgement. In the case of the discussed system this is purposeless – three available access levels provide satisfactory reserve (the highest, fourth level is reserved for the hardware monitoring console).

Because the µp card has access level on exclusive principle, bus request can be constantly active (BR2 = 0). Detailed comments of the state machine logic are marked directly on figure 1. It should only be noted that after system resetting the card does not take over the bus if at least single access has not been done by it. Such a strategy is a necessary condition for proper operation of multiprocessor system (many cards).

3. TRANSFER FORMAT MATCHING

An eight-byte data bus is phenomenal among microprocessors which with such wide transfers use binary equalization. Pentium processors implement 1, 2, 4, 8 bit transfers but start from an arbitrary address – possible supplementing cycles resulting from this are starting from addresses divisible by 8. This gives rise to eight signals, BE0/7, acknowledging utilisation of a given byte.

The standard of VMEbus admits an arbitrary configuration of bytes within a 32-bit word, which can be explained by its history. However 4/8 byte transfers already have to be binary aligned.

In the first version of the card attempts were made to reduce all transfer formulas (fig. 3a). An 8-bit cycle was temporarily divided in two, holding up cycle completion by µp. In the two subcycles DTACK acknowledgement signal was received twice with the AS signal confirming in each subcycle the validity of the original address, increased later by 4. For a VMEbus these are cycles using #0E or #0D modifiers. In the case when µp performed a block cycle it was combined not from four, but from eight data transfer stages which corresponded to the modifier having #0F value. These are, by the way, only “supervisor” type modifiers, because Intel does not specify an external current priority level.

Division of cycles did not prove to be a good solution in terms of educational purposes and caused significant complication of bus cycle state machine. The alternative was to assume that binary equalization would be kept. This can be, so to speak, forced by means of setting AM bit in CR0 register and AC bit in flags register. Transfer without binary alignment will now result in exception no. 17. This really applies only to data but code loading by µp always follows in the form
of equalized block transfer (32 bytes), which corresponds to capacity of line in cache memory.

The above solution (figure 3b) involves more buffers but significantly simplifies control. Such a solution employs cycles with #0C modifiers (line transfer) supplemented with #0D and #0E cycles. When accessing a simple 8-byte argument (for example: floating-point numbers), we use a multiplexed cycle also with #0C modifier but only once.

Fig. 3. Data transfer methods: a) cycle division, b) MBLT multiplexed cycle

It should be noted that the activity of each data bus buffer depends on the BB signal. It is generated by bus access state machine when card access to the bus is possible without conflicts. In the case of the address bus the situation is different. After releasing the bus μP goes to address tracing mode in order to enable
undertaking of actions leading to coherence of its cache memory contents with the main memory. Therefore the BB signal inverts direction of address bus buffers. The first version of the card also featured the above solution.

4. BUS CYCLE STATE MACHINE

Operations network (figure 4) was time optimised.

![Operations network of bus cycle state machine](image)

The states within the algorithm cycle were selected in such a way so that only one change of signal controlling VMEbus cycle took place for each clock cycle CLK. Condition AT is in fact an “aggregate”. Transfer acceptance takes place when:

a. system card has carried out acknowledgement prior to time-out elapsing

b. time-out system has operated
Additional acknowledgement in both cases is required from console (DTACKe signal).

BURST condition is produced for $\text{BURST} = \overline{\text{CACHE}} \cdot \overline{\text{KEN}} \lor \overline{\text{M/IO}} \cdot \overline{\text{W/R}}$ \text{CACHE} function which is inactive at single 8-byte access. Because $\mu$p does not inform about the end of the block cycle, LB condition creates an internal counter. Bus cycle state machine is accompanied by time-out logic, which by means of ER signal informs $\mu$p that acknowledgement is missing. Because the exception connected with BUSCHK is optional, therefore the ER signal also causes generation of non-mascable interruption plus effective termination of not acknowledged bus cycle.

5. SUMMARY

The study framework does not allow for the presentation of all dedicated functional solutions. The card which has been discussed cooperates with the simultaneously completed memory module adapted to 8-byte transfers. Up to now the lack of an auxiliary card containing controllers of 16 bits located at $\text{FFFFFFF0}$-$\text{FFFFFFFFFF}$ where $\mu$p starts running, causes some hindrance. Figure 5 shows the processor card. Figure 6 shows memory card, cooperating with the processor.
The necessity of PCB modification was unavoidable during the start-up stage. Foreseeing such a possibility signal layers of the card were located as external ones leaving technological openings and fields for additional component assembling. It was decided to decentralize programmable circuits (of GAL type, programmable through ISP). Thanks to this the feeding of all control signals to a single PLD circuit was not necessary and with only two signal layers would have been unrealistic.

Educational set: processor, memory plus hardware access console has proven its usability during laboratory classes. In order to enable the creation of basic software it is necessary to build keyboard cards and first of all – a screen monitor adapted to 8-byte transfers.

Accumulated experiences enable the undertaking of further actions aimed at creating a card with a Pentium 4 processor—obviously at an adequately low bus frequency.

REFERENCES


